

MxP – Media Express Processor for VoIP Networks

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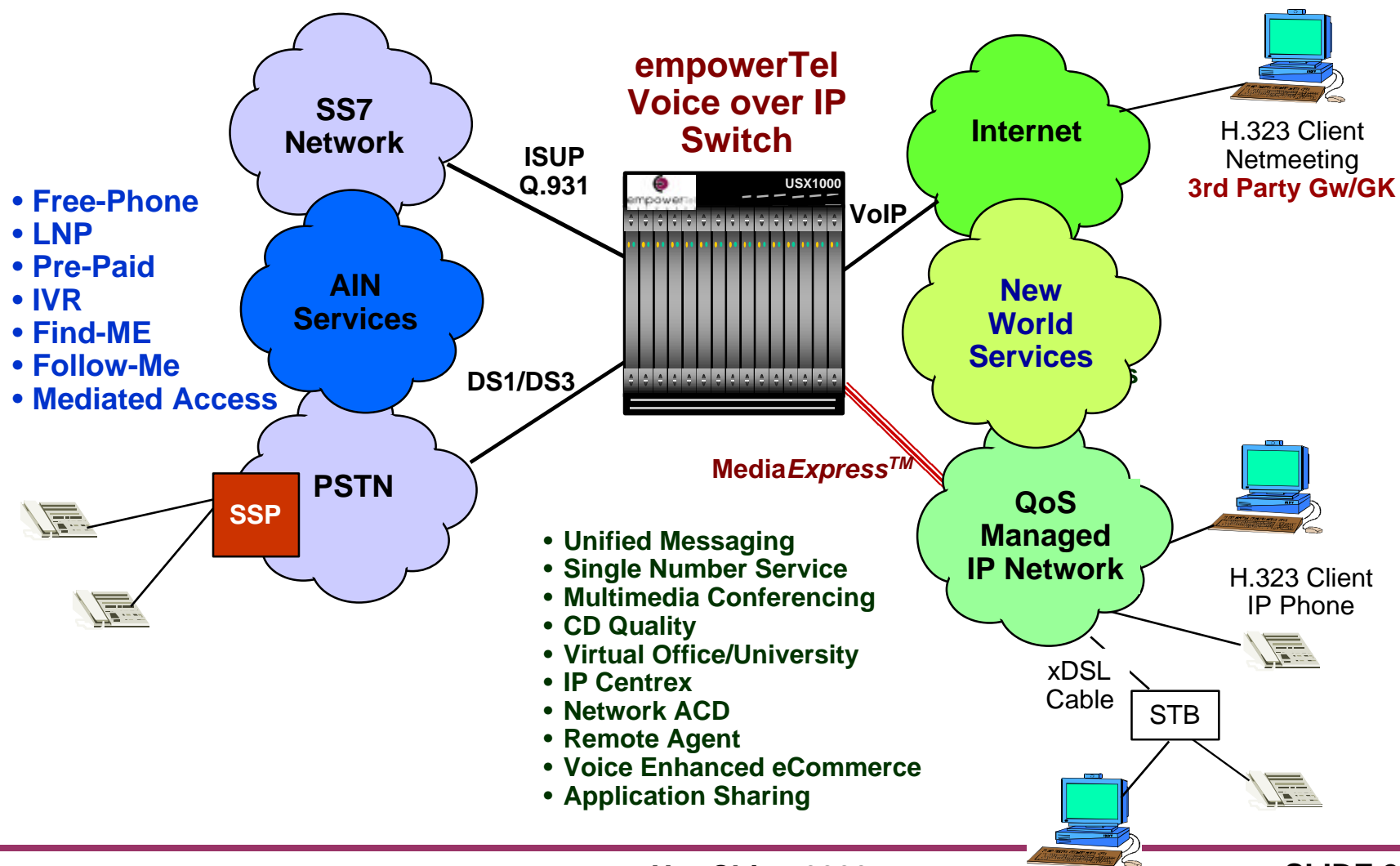
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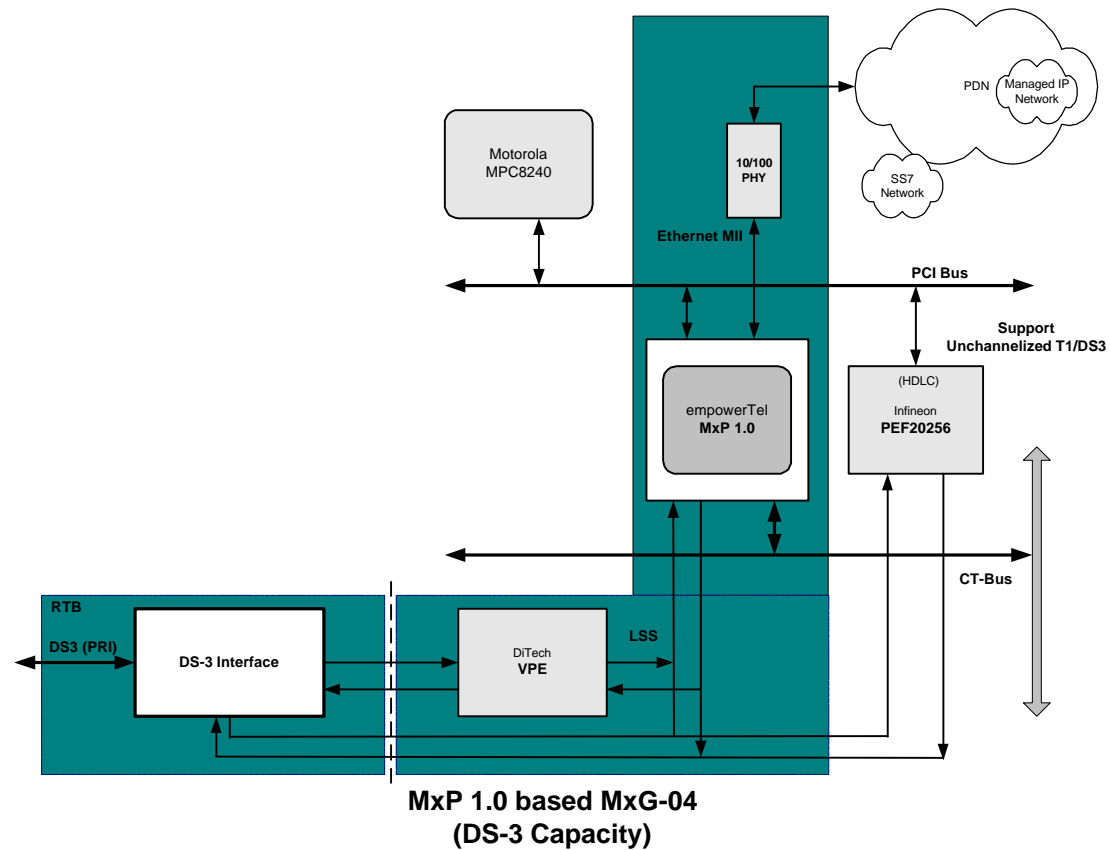
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empowered Network



MxP-based DS3 Board



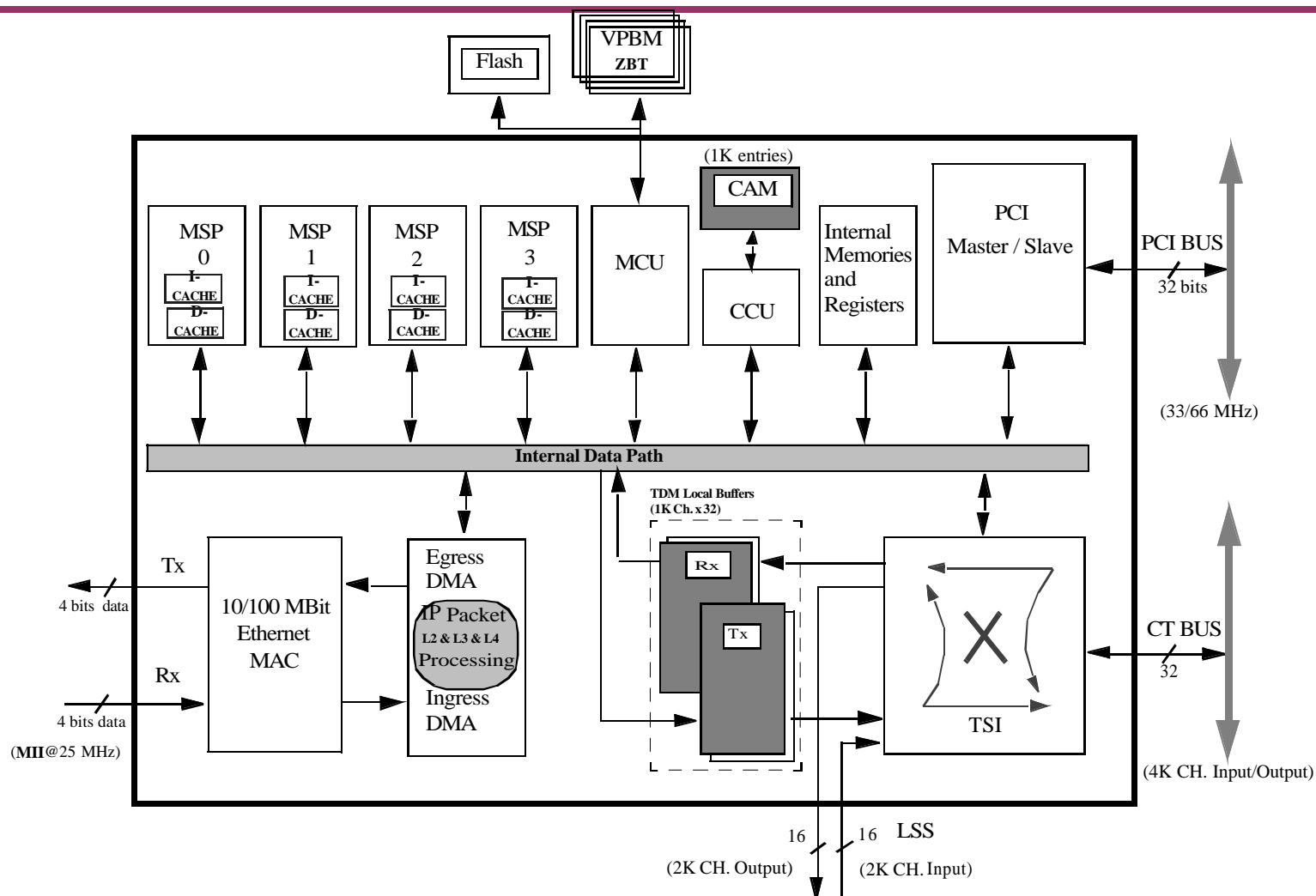
MxP Features

- High-performance and high-capacity TDM/IP packet processing
- Industry standard interfaces
 - PCI Bus, Revision 2.2
 - H.100/H.110 CT Bus
 - IEEE 802.3 - Media Independent Interface (MII)
 - IEEE 1149.1 - Test Access Port and Boundary Scan (JTAG)
 - Compact PCI Hot Swap
- Four embedded Media Stream Processors (MSPs)
- Hardware assist for processing IP/UDP/RTP headers on Ethernet Receive Packets

MxP Features (cont'd)

- Embedded VoIPCAM Core for fast lookups with constant latency – $O(1)$
- Jitter Buffer Valid Bits for keeping track of valid voice samples in the Jitter Buffer Memory
- Large Time Slot Interchanger (TSI) to support CT Bus and Local Serial Streams for DS3 capacity
- Echo cancellation, voice activity detection, voice compression, DTMF, etc. supported by MSPs/external DSPs through CT Bus and/or Local Serial Streams
- Mailboxes for inter-processor communication

MxP Block Diagram



Media Stream Processors

- Four embedded MIPS32 4Km Processors
- Two cache configurations
 - 16KB I-Cache, 2KB D-Cache
 - 8KB I-Cache, 4KB D-Cache
- Executes 'Media Flow' code
- Collects metrics for supporting RTCP and implementing Quality of Service features - weighted fair queuing, weighted early discard

Layer Processor

- Hardware acceleration for packet reception
- Performs checksum on packet and checks for status errors
- Filters IP/UDP/RTP voice packets to be processed by a Media Stream Processor
- Pre-processes the IP/UDP/RTP header and aligns the payload to accelerate processing for the Media Stream Processor

VoIPCAM

- Embedded Content Addressable Memory
- Supports up to 1024 channels
- Constant latency - $O(1)$ for search operations
- 128-deep FIFO can store search results for the maximum number of channels in a Multiplexed RTP packet; allows search operations to the VoIPCAM to be pipelined

Jitter Buffer Valid Bits

- Keeps track of valid voice samples in the Jitter Buffer
- Shadows Jitter Buffer Memory accesses
- Bit is set when Jitter Buffer is written; reset when Jitter Buffer is read
- Loss data recovery can be implemented when Jitter Buffer does not contain valid data; repeat playout of last voice sample or generate data based on last few voice samples

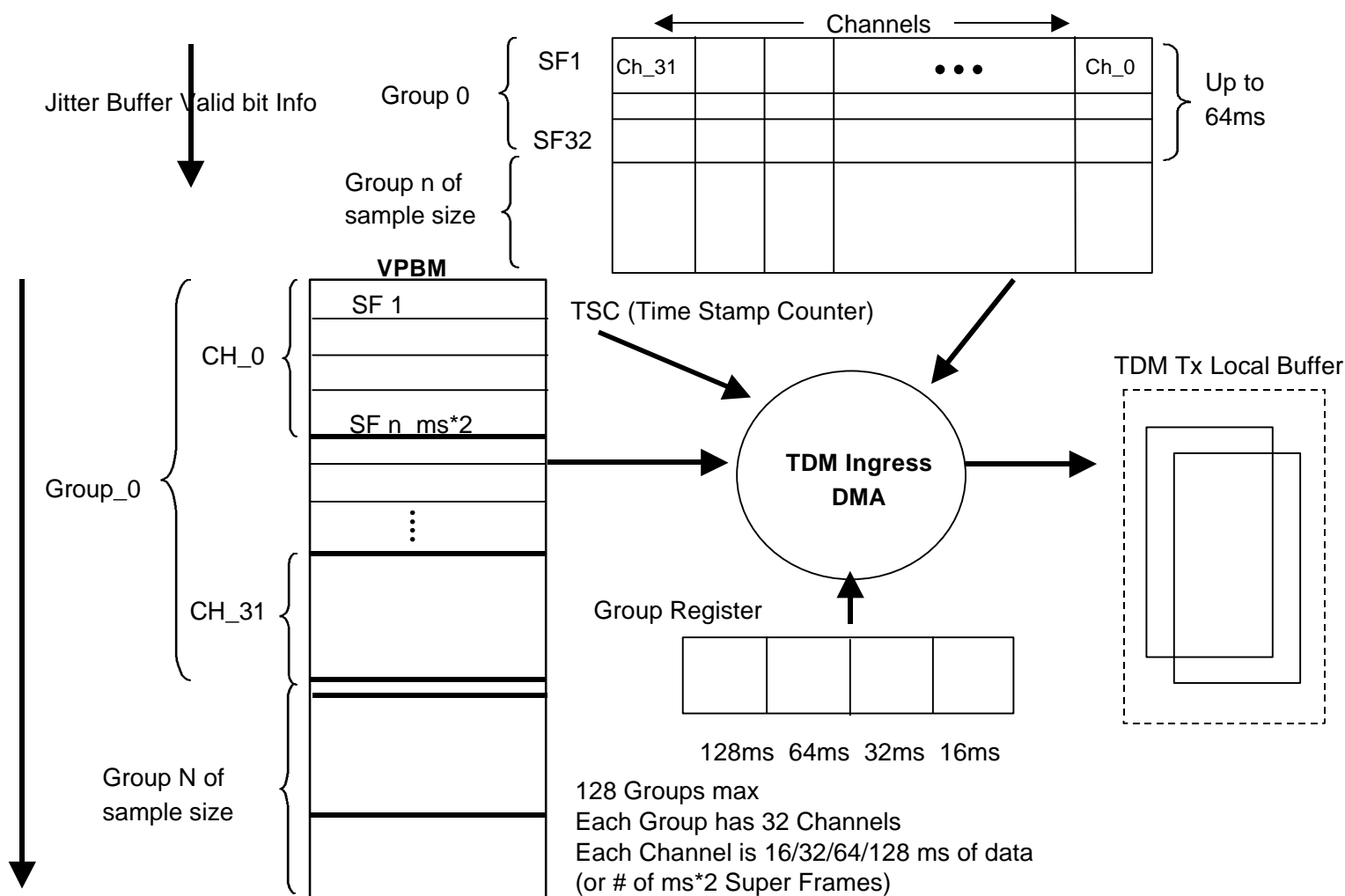
Gateway Software

- Gateway enables PSTN convergence over Public Data Networks
- Convergence requires Transport & Signaling
- Media Flow and Media Express Processor (MxP) – Transport GW between TDM & IP
- Media Flow converts between TDM voice samples and IP packets, and vice versa
- Media Flow runs on the Local Processor & MSPs
- Shared Memory paradigm

Media Flow Design

- **Egress Media Flow - TDM to IP**
 - Move data from TDM Receive Buffer to payload buffers (every 0.5 ms).
 - Packetize and transmit using the Transmit DMA (TDM Egress DMA).
- **Ingress Media Flow - IP to TDM**
 - Receive packets from Ethernet. Layer Processor Hardware distinguishes RTP vs. non-RTP packets.
 - Extract voice payload from RTP packet. Write data to Jitter Buffer (MSP).
 - Playout voice data by writing data to the TDM Transmit Buffer (MSP/TDM Ingress DMA).

TDM Ingress Data Flow

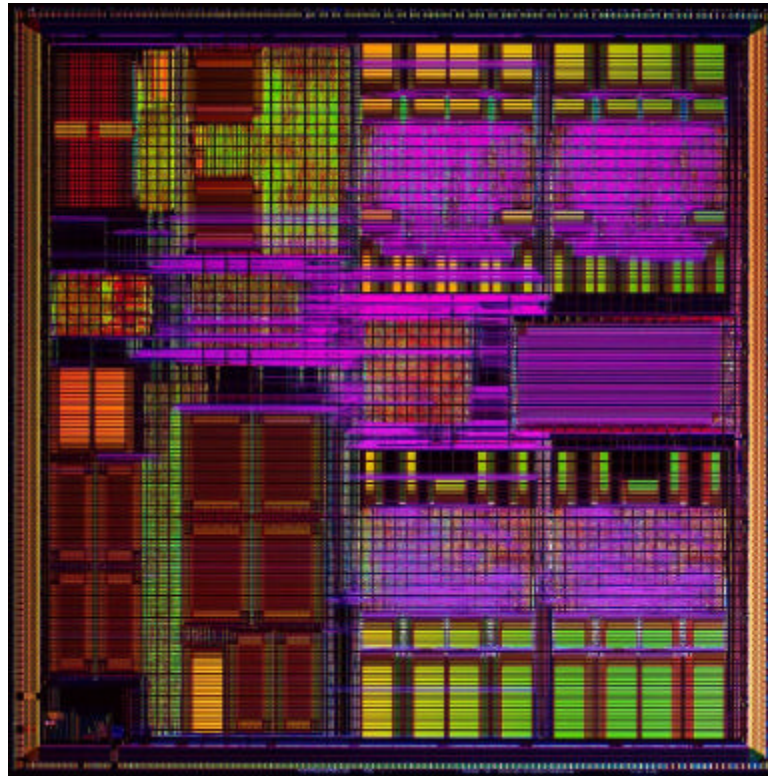




MxP Physical Data

- TSMC 0.25 um technology (one poly, 5 metals)
- 115 MHz (worst process, 2.25 volts, 125 degree C)
- Fault coverage for the full chip 98.65%
- 13.5 million transistors
- 10.93 mm x 10.93 mm die size
- 388 pin BGA (4-layer substrate) with an internal heat slug and an external heat sink.
- 7 watts

MxP Die Photo



Future Research and Development

- Increase capacity to multiple OC-3s
- Terminate VoDSL traffic
 - Convergence between Narrowband, Broadband, and Network Core (Unified Network)
- Integrate high-capacity echo cancellation, voice activity detection, voice compression solutions
- Transport agnostic network interface